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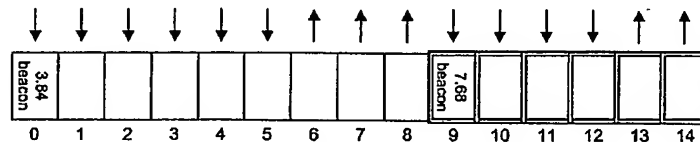
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(54) Title: SUPPORT OF PLURAL CHIP RATES IN A CDMA SYSTEM



key



lower chip rate (3.84Mcps) timeslot



higher chip rate (7.68Mcps) timeslot

400

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(57) Abstract: In a CDMA system (100), two chip rates in a TDD cell are supported by: transmitting signals in the system in a frame (400) having a plurality of timeslots; operating at least a first one (0-8) of the plurality of timeslots in the frame at a lower chip rate; and operating at least a second one (9-14) of the plurality of timeslots in the frame at a higher chip rate. This provides the following advantages: provides backwards compatibility of a network including higher chip rate functionality with existing lower chip rate user equipment; allows greater network capacity during the transition phase from a low chip rate network to a high chip rate network; and allows a network operator with a high chip rate network to provide service to roaming users from low chip rate networks.